Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-4 (Canceled)

Claim 5 (New): An operational amplifier comprising:

a step-up circuit supplied with a first voltage, the step-up circuit providing a second voltage which is higher than the first voltage;

a differential input circuit that provides a differential voltage signal, the differential input circuit including

a first transistor having a first electrode supplied with the second voltage and a second electrode,

a second transistor that receives a first input signal, the second transistor having a first electrode coupled to the second electrode of the first transistor and a second electrode,

a third transistor that receives a second input signal, the third transistor having a first electrode coupled to the second electrode of the first transistor and a second electrode,

a fourth transistor having a first electrode coupled to the second electrode of the second transistor and a second electrode supplied with a third voltage which is lower than the first voltage, and

a fifth transistor having a first electrode coupled to the second electrode of the third transistor and a second electrode supplied with the third voltage; and

an output circuit supplied with the first voltage, wherein the output circuit receives the differential voltage signal.

Claim 6 (New): The operational amplifier of claim 5, wherein the differential input circuit further comprises:

a sixth transistor having a first electrode, a second electrode supplied with the third voltage, and a gate electrode coupled to a gate electrode of the fourth transistor and to the second electrode of the second transistor, the fourth and sixth transistors being configured as a first current mirror; and

a seventh transistor having a first electrode coupled to a first node, a second node coupled to the third voltage, and a gate electrode coupled to a gate electrode of the fifth transistor and to the second electrode of the third transistor, the fifth and seventh transistors being configured as a second current mirror circuit.

Claim 7 (New): The operational amplifier of claim 6, wherein the output circuit comprises:

an eighth transistor having a first electrode coupled to a second node, a second electrode coupled to the third voltage, and a gate electrode coupled to the first node; and

a ninth transistor having a first electrode supplied with the first voltage and a second electrode coupled to the second node,

an output of the operational amplifier being provided via the second node.

Claim 8 (New): The operational amplifier of claim 7, further comprising an amplifying circuit including:

a tenth transistor having a first electrode coupled to a third node, a second electrode coupled to the third voltage, and a gate electrode coupled to the first node; and

an eleventh transistor having a first electrode coupled to the second voltage, a second electrode coupled to the third node, and a gate electrode having a bias voltage supplied thereto, a gate of the ninth transistor being coupled to the third node.

Claim 9 (New): The operational amplifier of claim 8, wherein the first through third and eleventh transistors are first conductivity type transistors, and the fourth through tenth transistors are second conductivity type transistors that have conductivity type opposite the first conductivity type transistors.

Claim 10 (New): The operational amplifier of claim 9, wherein the first conductivity type transistors are p-channel transistors and the second conductivity type transistors are n-channel transistors.

Claim 11 (New): The operational amplifier of claim 7, wherein the first through third transistors are first conductivity type transistors, and the fourth through ninth transistors are second conductivity type transistors that have conductivity type opposite the first conductivity type transistors.

Claim 12 (New): The operational amplifier of claim 11, wherein the first conductivity type transistors are p-channel transistors and the second conductivity type transistors are n-channel transistors.

Claim 13 (New): The operational amplifier of claim 5, wherein the first through third transistors are first conductivity type transistors, and the fourth and fifth transistors are second conductivity type transistors that have conductivity type opposite the first conductivity type transistors.

Claim 14 (New): The operational amplifier of claim 13, wherein the first conductivity type transistors are p-channel transistors and the second conductivity type transistors are n-channel transistors.

Claim 15 (New): The operational amplifier of claim 5, wherein the step-up circuit comprises:

a voltage doubler rectifier that generates a dc voltage several times as large as the first voltage;

a capacitor that stores the dc voltage;

a first node connected between the voltage doubler rectifier and the capacitor; and

a clamp that clamps a voltage at the first node to provide the clamped voltage as the second voltage output from the first node.

Claim 16 (New): An operational amplifier comprising:

a differential amplifier circuit which includes a first transistor coupled to a first input terminal, a second transistor coupled to a second input terminal, a third transistor coupled to the first and second transistors, a fourth transistor coupled to the first transistor and a ground, and a fifth transistor coupled to the second transistor, a first node and the ground;

a step-up circuit coupled to the third transistor and a second node supplied with a first voltage, the step-up circuit providing to the third transistor a second voltage which is higher than the first voltage; and

an output circuit coupled to the first node, the second node and an output

terminal of the operational amplifier.

Claim 17 (New): The operational amplifier of claim 16, wherein the output circuit comprises:

a sixth transistor coupled to the first node and between the ground and the output terminal; and

a seventh transistor coupled between the second node and the output terminal.

Claim 18 (New): The operational amplifier of claim 17, further comprising an amplifying circuit including:

an eighth transistor coupled to the first node and between a third node and the ground; and

a ninth transistor coupled to a bias voltage, and between the second voltage and the ground, a gate of the seventh transistor being coupled to the third node.

Claim 19 (New): The operational amplifier of claim 18, wherein the first through third and ninth transistors are first conductivity type transistors, and the fourth through eighth transistors are second conductivity type transistors having conductivity type opposite the first conductivity type transistors.

Claim 20 (New): The operational amplifier of claim 19, wherein the first conductivity type

transistors are p-channel transistors and the second conductivity type transistors are n-channel transistors.

Claim 21 (New): The operational amplifier of claim 16, wherein the first through third transistors are first conductivity type transistors, and the fourth and fifth transistors are second conductivity type transistors having conductivity type opposite the first conductivity type transistors.

Claim 22 (New): The operational amplifier of claim 21, wherein the first conductivity type transistors are p-channel transistors and the second conductivity type transistors are n-channel transistors.

Claim 23 (New): The operational amplifier of claim 16, wherein the differential amplifier further comprises:

a sixth transistor coupled to the fourth transistor and the ground, the fourth and sixth transistors being configured as a first current mirror; and

a seventh transistor coupled to the fifth transistor and between the first node and the ground, the fifth and seventh transistors being configured as a second current mirror.

Claim 24 (New): The operational amplifier of claim 16, wherein the step-up circuit

comprises:

a voltage doubler rectifier that generates a dc voltage several times as large as the first voltage;

a capacitor that stores the dc voltage,

the second node being connected between the voltage doubler rectifier and the capacitor; and

a clamp that clamps a voltage at the second node to provide the clamped voltage as the second voltage output from the second node.